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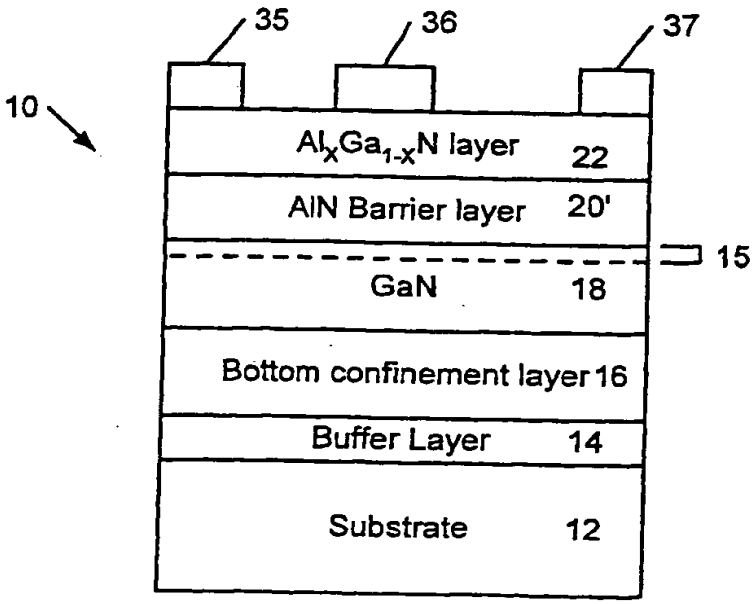

(57) Abstract: A nitride based heterojunction transistor includes a substrate and a first Group III nitride layer, such as an AlGaN based layer, on the substrate. The first Group III-nitride based layer has an associated first strain. A second Group III-nitride based layer, such as a GaN based layer, is on the first Group III-nitride based layer. The second Group III-nitride based layer has a bandgap that is less than a bandgap of the first Group III-nitride based layer and has an associated second strain. The second strain has a magnitude that is greater than a magnitude of the first strain. A third Group III-nitride based layer, such as an AlGaN or AlN layer, is on the GaN layer. The third Group III-nitride based layer has a bandgap that is greater than the bandgap of the second Group III-nitride based layer and has an associated third strain. The third strain is of opposite strain type to the second strain. A source contact, a drain contact and a gate contact may be provided on the third Group III-nitride based layer. Nitride based heterojunction transistors having an AlGaN based bottom confinement layer, a GaN based channel layer on the bottom confinement layer and an AlGaN based barrier layer on the channel layer, the barrier layer having a higher concentration of aluminum than the bottom confinement layer, are also provided. Methods of fabricating such transistor are also provided.

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STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTORS AND METHODS OF FABRICATING STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTORS

RELATED APPLICATIONS

The present application is related to and claims priority from United States Provisional Application Serial No. 60/337,687, filed December 3, 2001 and entitled "*Strain Balanced Nitride Heterojunction Transistor*" the disclosure of which is incorporated herein as if set forth fully herein.

FIELD OF THE INVENTION

The present invention relates to high frequency transistors and in particular relates to a high electron mobility transistor (HEMT) that incorporates nitride-based active layers.

BACKGROUND

The present invention relates to transistors formed of semiconductor materials that can make them suitable for high power, high temperature, and/or high frequency applications. Materials such as silicon (Si) and gallium arsenide (GaAs) have found wide application in semiconductor devices for lower power and (in the case of Si) lower frequency applications. These, more familiar, semiconductor materials may not be well suited for higher power and/or high frequency applications, however, because of their relatively small bandgaps (*e.g.*, 1.12 eV for Si and 1.42 for GaAs at room temperature) and/or relatively small breakdown voltages.

In light of the difficulties presented by Si and GaAs, interest in high power, high temperature and/or high frequency applications and devices has turned to wide bandgap semiconductor materials such as silicon carbide (2.996 eV for alpha SiC at room temperature) and the Group III nitrides (*e.g.*, 3.36 eV for GaN at room temperature). These materials, typically, have higher electric field breakdown strengths and higher electron saturation velocities as compared to gallium arsenide and silicon.

A device of particular interest for high power and/or high frequency applications is the high electron mobility transistor (HEMT), which is also known as a modulation doped field effect transistor (MODFET). These devices may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity. The 2DEG is an accumulation layer in the undoped, smaller bandgap material and can contain a very high sheet electron concentration in excess of, for example, 10^{13} carriers/cm^2. Additionally, electrons that originate in the wider-bandgap semiconductor transfer to the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering.

This combination of high carrier concentration and high carrier mobility can give the HEMT a very large transconductance and may provide a strong performance advantage over metal-semiconductor field effect transistors (MESFETs) for high-frequency applications.

High electron mobility transistors fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material system have the potential to generate large amounts of RF power because of the combination of material characteristics that includes the aforementioned high breakdown fields, their wide bandgaps, large conduction band offset, and/or high saturated electron drift velocity. A major portion of the electrons in the 2DEG is attributed to polarization in the AlGaN. HEMTs in the GaN/AlGaN system have already been demonstrated. U.S. Patents 5,192,987 and 5,296,395 describe AlGaN/GaN HEMT structures and methods of manufacture. U.S. Patent No. 6,316,793, to Sheppard et al., which is commonly assigned and is incorporated herein by reference, describes a HEMT device having a semi-insulating silicon carbide substrate, an aluminum nitride buffer layer on the substrate, an insulating gallium nitride layer on the buffer layer, an aluminum gallium nitride barrier layer on the gallium nitride layer, and a passivation layer on the aluminum gallium nitride active structure.

One limiting factor in the design of nitride-based HEMTs may be the aluminum concentration and thickness of the AlGaN barrier layer. In order to increase or maximize carrier concentration in the channel layer, it is desirable to have a relatively thick AlGaN barrier layer having a relatively high aluminum content. As described above, the AlGaN barrier layer is the source of carriers in the two

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dimensional electron gas. Accordingly a thicker barrier layer can supply more carriers to the channel. In addition, thicker AlGaN layers with higher aluminum compositions are capable of producing larger piezoelectric fields and more spontaneous charge, that contribute to the formation of the two dimensional electron gas with high carrier concentration. However, thick AlGaN layers with high aluminum content tend to crack either during growth or after cooling, which destroys the device.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide a nitride based heterojunction transistor including a substrate and a first AlGaN based layer on the substrate. The first AlGaN based layer has an associated first strain energy. A GaN based layer is on the first AlGaN based layer. The GaN based layer has a bandgap that is less than a bandgap of the first AlGaN based layer and has an associated second strain energy. The second strain energy has a magnitude that is greater than a magnitude of the first strain energy. A second AlGaN based layer is on the GaN layer. The second AlGaN based layer has a bandgap that is greater than the bandgap of the GaN based layer and has an associated third strain energy. The third strain energy is of opposite strain type to the second strain energy. A source contact, a drain contact and a gate contact may also be provided on the second AlGaN based layer.

In additional embodiments of the present invention, an AlN layer is provided on the GaN based layer and disposed between the GaN based layer and the second AlGaN based layer. In certain embodiments, the first AlGaN based layer is a short period super-lattice of AlN based layers and GaN based layers. In such embodiments, the AlN based layers and the GaN based layers of the short period super-lattice may be AlN layers and GaN layers respectively. The second AlGaN based layer may also be an $Al_xGa_{1-x}N$ layer, where $0 < x \leq 1$.

In further embodiments of the present invention, the first AlGaN based layer is a bottom confinement layer, the GaN layer is a channel layer and the second AlGaN based layer is a barrier layer. In further embodiments, the bottom confinement layer has a first aluminum concentration and the barrier layer has a second aluminum concentration different from the first aluminum concentration. The second aluminum concentration may be greater than the first aluminum concentration.

In additional embodiments of the present invention, the second AlGaN based layer has a thickness and aluminum concentration large enough to induce formation of a 2D electron gas at the interface with the GaN based layer, but less than a thickness at which cracking or defect formation occurs. In particular embodiments of the present invention, the second AlGaN layer has a thickness of at least about 10 nm.

In other embodiments of the present invention, the total strain energy in the first AlGaN based layer, the GaN based layer and the second AlGaN based layer at a growth temperature is approximately zero.

In still further embodiments of the present invention, the first AlGaN based layer, the GaN layer and the second AlGaN based layer are substantially coherently strained in the "a" crystal lattice direction.

In additional embodiments of the present invention, a buffer layer is provided between the substrate and the first AlGaN based layer. The buffer layer may be an AlN layer.

In other embodiments of the present invention, the GaN based layer is directly on the first AlGaN based layer. The second AlGaN based layer may also be directly on the GaN based layer. The first AlGaN based layer may be a graded AlGaN based layer. The first AlGaN based layer may also be an AlGaN layer. Alternatively, the first AlGaN based layer may be an AlInGaN layer.

In certain embodiments of the present invention, the first AlGaN based layer has an aluminum percentage of greater than about 10%. The second AlGaN based layer may also have an aluminum percentage of greater than about 20%. The first AlGaN based layer may have a thickness of at least about 1000nm. The GaN based layer may have a thickness of from about 30 Å to about 300 Å. Alternatively, the GaN based layer may have a thickness of greater than about 500 Å. Furthermore, in certain embodiments, the substrate may be a silicon carbide substrate, a sapphire substrate, an AlN substrate and/or a silicon substrate.

In further embodiments of the present invention, a method of fabricating a nitride based heterojunction transistor is provided by forming a substantially unstrained AlGaN based layer on a substrate, forming a compressive strained GaN based layer on the substantially unstrained AlGaN based layer and forming a tensile strained AlGaN based layer on the compressive strained GaN based layer. The tensile strained AlGaN based layer may be formed having a predefined tensile strain on the compressive strained GaN based layer. The predefined tensile strain may provide a

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tensile strain such that a total strain energy of the compressive strained GaN based layer and the tensile strained AlGaN based layer is about zero. The predefined tensile strain may be provided by adjusting the thickness of the tensile strained AlGaN based layer, a composition of the substantially unstrained AlGaN based layer and/or an aluminum concentration in the tensile strained AlGaN based layer to provide the predefined tensile strain.

In additional embodiments of the present invention, the substantially unstrained AlGaN based layer is formed by forming three dimensional islands of AlGaN based material on the substrate and growing the AlGaN based material so that the AlGaN based material coalesces between the three dimensional islands to provide the substantially unstrained AlGaN based layer. The substantially unstrained AlGaN based layer may be a substantially unstrained AlGaN layer. Alternatively, the substantially unstrained AlGaN based layer may be a substantially unstrained AlInGaN layer. The tensile strained AlGaN based layer may be a tensile strained AlGaN layer. Alternatively, the tensile strained AlGaN based layer may be a tensile strained AlInGaN layer. Furthermore, the tensile strained AlGaN based layer may have a thickness of at least 10 nm. The compressive strained GaN based layer may have a thickness of from about 30 Å to about 300 Å. Alternatively, the compressive strained GaN based layer may have a thickness of greater than about 500 Å.

In still further embodiments of the present invention, the substantially unstrained AlGaN based layer is formed by forming a substantially unstrained AlGaN based layer having a first aluminum concentration and the tensile strained AlGaN based layer is formed by forming a tensile strained AlGaN based layer having a second aluminum concentration different from the first aluminum concentration. In particular embodiments, the second aluminum concentration is greater than the first aluminum concentration. Furthermore, the tensile strained AlGaN based layer may be provided by forming a tensile strained AlGaN based layer having a thickness and aluminum concentration large enough to induce formation of a 2D electron gas at the interface with the compressive strained GaN based layer, but less than a thickness at which cracking or defect formation occurs.

In additional embodiments of the present invention, a nitride based heterojunction transistor includes an AlGaN based bottom confinement layer, a GaN based channel layer on the bottom confinement layer and an AlGaN based barrier layer on the channel layer. The barrier layer has a higher concentration of aluminum

than the bottom confinement layer. The channel layer may have a thickness of from about 30 Å to about 300 Å. The barrier layer may have a thickness of at least about 10 nm. The bottom confinement layer may be provided, for example, on a silicon carbide substrate, a sapphire substrate, an AlN substrate and/or a silicon substrate. An AlN buffer layer between the silicon carbide substrate and the bottom confinement layer may also be provided. The bottom confinement layer may also be a graded AlGaN based layer. A GaN based contact layer may be provided on the barrier layer. The bottom confinement layer and the barrier layer may each have an aluminum concentration of greater than about 10%. Methods of fabricating such transistors are also provided.

In still further embodiments of the present invention, a Group III-nitride based heterojunction transistor structure is provided having a substrate and a first Group III-nitride based layer on the substrate, the first Group III-nitride based layer having a first strain associated therewith. A second Group III-nitride based layer is on the first Group III-nitride based layer. The second Group III-nitride based layer has a bandgap that is less than a bandgap of the first Group III-nitride based layer and has a second strain associated therewith. The second strain has a magnitude that is greater than a magnitude of the first strain. A third Group III-nitride based layer is on the second Group III-nitride based layer opposite the first Group III-nitride based layer. The third Group III-nitride based layer has a bandgap that is greater than the bandgap of the second Group III-nitride based layer and has a third strain associated therewith, the third strain being of opposite strain type to the second strain. In additional embodiments of the present invention, the first Group III-nitride based layer is an $Al_xGa_{1-x}N$ layer, where $0 < x \leq 1$. The second Group III-nitride based layer may be a GaN layer. The third Group III-nitride base layer may be an AlN layer. Methods of fabricating such transistors are also provided.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic drawing showing a transistor according to embodiments of the present invention.

Figure 2 is a diagram of the band energy of an embodiment of the present invention.

Figure 3 is a diagram of a prior art HEMT structure.

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Figure 4 is a schematic drawing showing a transistor according to further embodiments of the present invention.

DETAILED DESCRIPTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Furthermore, the various layers and regions illustrated in the figures are illustrated schematically. Accordingly, the present invention is not limited to the relative size and spacing illustrated in the accompanying figures. As will also be appreciated by those of skill in the art, references herein to a layer formed "on" a substrate or other layer may refer to the layer formed directly on the substrate or other layer or on an intervening layer or layers formed on the substrate or other layer.

Embodiments of the present invention are schematically illustrated as a high electron mobility transistor (HEMT) **10** in the cross-sectional view of **Figure 1**. The transistor **10** includes a semi-insulating silicon carbide (SiC) substrate **12** that may be, for example, 4H polytype of silicon carbide. Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes. The term "semi-insulating" is used descriptively rather than in an absolute sense. In particular embodiments of the present invention, the silicon carbide bulk crystal has a resistivity equal to or higher than about $1x10^5$ Ω-cm at room temperature.

An optional aluminum nitride buffer layer **14** is on the substrate **12** and provides an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Silicon carbide has a much closer crystal lattice match to Group III nitrides than does sapphire (Al_2O_3), which is a very common substrate material for Group III nitride devices. The closer lattice match may result in Group III nitride films of higher quality than those generally available on sapphire. Silicon carbide also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is, typically, not as limited by thermal dissipation of the substrate as in the case of the same devices

formed on sapphire. Also, the availability of semi-insulating silicon carbide substrates may provide for device isolation and reduced parasitic capacitance.

Although silicon carbide is the preferred substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like. In some embodiments, an appropriate buffer layer also may be formed.

As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). The term also refers to ternary and quaternary compounds such as AlGaN and AlInGaN. As is well understood by those in this art, the Group III elements can combine with nitrogen to form binary (*e.g.*, GaN), ternary (*e.g.*, AlGaN, AlInN), and quaternary (*e.g.*, AlInGaN) compounds. These compounds all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the Group III elements. Accordingly, formulas such as $Al_xGa_{1-x}N$ where $0 \leq x \leq 1$ are often used to describe them.

Appropriate SiC substrates are manufactured by, for example, Cree, Inc., of Durham, N.C., the assignee of the present invention, and the methods for producing are described, for example, U. S. Patent Nos. Re. 34,861; 4,946,547; 5,200,022; and 6,218,680, the contents of which are incorporated herein by reference in their entirety. Similarly, techniques for epitaxial growth of Group III nitrides have been described in, for example, U. S. Patent Nos. 5,210,051; 5,393,993; 5,523,589; and 5,292,501, the contents of which are also incorporated herein by reference in their entirety. Suitable structures for GaN-based HEMTs are described, for example, in commonly assigned U.S. Patent 6,316,793 and U.S. application serial no. 09/904,333 filed July 12, 2001 for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," U.S. provisional application serial no. 60/290,195 filed May 11, 2001 for "GROUP III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" and United States Patent Application Serial No. 10/102,272, to Smorchkova *et al.*, entitled "GROUP-III

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NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosures of which are hereby incorporated herein by reference in their entirety.

Returning to **Figure 1**, the transistor **10** includes a bottom confinement layer **16** and a channel layer **18**. The bottom confinement layer **16** has a bandgap larger than that of channel layer **18**. In certain embodiments of the present invention, the bottom confinement layer **16** has a substantially lower strain energy than that of the channel layer **18** and may be substantially relaxed (*i.e.* substantially unstrained). For example, the bottom confinement layer may have a strain that is about 0 or may have a strain that is from about 0 to about 100% the strain of the channel layer **18**. In certain embodiments of the present invention, the bottom confinement layer **16** has a stress of less than about 1 GPa. In some embodiments of the present invention, the bottom confinement layer **16** may comprise a Group III-nitride, such as AlGaN or AlInGaN and the AlGaN and AlInGaN may be substantially free of dopants, such as Si and Mg. The bottom confinement layer **16** may be at least about 1000 nm thick, but is not so thick as to cause cracking or defect formation therein. The bottom confinement layer **16** may be semi-insulating. In certain embodiments, the bottom confinement layer **16** is AlGaN with a substantially uniform aluminum concentration between about 1% and 100%, and preferably greater than 10%. Alternatively, the bottom confinement layer **16** may be graded with an increasing, decreasing and/or increasing and decreasing aluminum concentration to better match the lattice constant of the channel layer **18**. The bottom confinement layer **16** may also be a short period super-lattice of alternating layers of AlN and GaN. The term AlGaN based layer may also refer to a super-lattice of AlN and GaN and/or AlGaN and AlN and/or GaN.

The bottom confinement layer **16** may be fabricated as a substantially relaxed layer by forming three dimensional islands on the substrate **12** or the buffer layer **14** and growing the bottom confinement layer **16** such that the AlGaN based material coalesces between the islands. Such growth can provide an AlGaN based layer that is substantially relaxed and does not take on the lattice constant of the underlying substrate. Formation of larger islands may be beneficial in reducing tensile strain.

For example, in certain embodiments of the present invention a semi-insulating AlN layer is deposited at high temperature (>1000 °C) on a semi-insulating SiC substrate as a nucleation/buffer layer. Next, a semi-insulating $Al_xGa_{1-x}N$ layer (x~0.1-0.2) is deposited at high temperature (>1000 °C) on the AlN layer. The growth

conditions (such as temperature, pressure, V/III ratio, growth rate, thickness, etc.) are adjusted to ensure that the AlGaN is not coherently strained to the AlN layer. Preferably, the AlGaN will initially begin growth in a three-dimensional mode with a relatively low density of nuclei ($<10^9$ cm^{-2}). As would be appreciated by those of skill in the art in light of the present disclosure, the detailed growth conditions may differ depending on reactor geometry and, therefore, may be adjusted accordingly to achieve AlGaN with these properties.

In further embodiments, the $Al_xGa_{1-x}N$ layer is graded with composition x decreasing during the growth. Furthermore, the layers may be grown as described above, but without the AlN layer, such that the AlGaN is grown directly on the SiC substrate in a substantially relaxed manner as described above.

In addition to the optional buffer layer **14**, the bottom confinement layer **16** may be formed on or above one or more optional intervening layers (not shown). If such is the case, the strain energy that such intervening layers impart to the overall structure should be taken into account as described below.

In some embodiments of the present invention, the channel layer **18** is a Group III-nitride, such as $Al_xGa_{1-x}N$ where $0 \leq x < 1$, provided that the bandgap of the channel layer **18** is less than the bandgap of the bottom confinement layer **16**. In certain embodiments of the present invention, $x = 0$, indicating that the channel layer **18** is GaN. The channel layer **18** may be undoped and may be grown to a thickness of between about 30 and about 300 Å. Thus, the channel layer **18** may be thinner than those in conventional GaN HEMT devices, which are typically greater than 500 Å in thickness. Because of the confinement provided by the bottom confinement layer **16**, there may be less "tailing" of carriers into the GaN layer. Thus, the resulting devices may exhibit more linearity than devices found in the prior art. Alternatively, if strain control is a consideration and additional confinement is less of a consideration, the GaN channel layer **18** may be grown thicker than 500 Å and the aluminum percentage in the bottom confinement layer **16** may be reduced.

Furthermore, the interface between the bottom confinement layer **16** and the channel layer **18** may be doped n-type. For example, the portion of the bottom confinement layer **16** adjacent the channel layer may be doped to about 3×10^{12} cm^{-2}. Such a doping at the interface may counteract the positive charge at the interface. The

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channel layer **18**, or portions thereof adjacent the bottom confinement layer **16**, may also be doped n-type.

A barrier layer **20** is provided on the channel layer **18**. Like the bottom confinement layer **16**, the barrier layer **20** may be a Group III-nitride and has a bandgap larger than that of the channel layer **18** and may be tensile strained as described below. Accordingly, the barrier layer **20** may be AlGaN, AlInGaN and/or AlN. The barrier layer **20** may be at least about 10 nm thick, but is not so thick as to cause cracking or defect formation therein. Preferably, the barrier layer **20** is undoped or doped with a concentration less than about 10^{19} cm^{-3}. In some embodiments of the present invention, the barrier layer **20** is $Al_xGa_{1-x}N$ where $0 < x \leq 1$. In certain embodiments of the present invention, the barrier layer **20** comprises AlGaN with an aluminum concentration of between about 5% and about 100%. In specific embodiments of the present invention, the aluminum concentration is greater than about 10%. Furthermore, the aluminum concentration in the barrier layer **20** may be greater than the aluminum concentration in the bottom confinement layer **16**.

The barrier layer may also be provided with multiple layers as described in United States Patent Application Serial No. 10/102,272, to Smorchkova *et al.*, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosure of which is incorporated herein by reference as if set forth fully herein. Thus, embodiments of the present invention should not be construed as limiting the barrier layer to a single layer but may include, for example, barrier layers having combinations of GaN, AlGaN and/or AlN layers. For example, a GaN, AlN structure may be utilized to reduce or prevent contamination of the GaN layers by contact material that may result in alloy scattering. An example of a structure according to further embodiments of the present invention is illustrated in **Figure 4**, where an AlN nitride barrier layer **20'** is provided on the GaN based layer **18** and an $Al_xGa_{1-x}N$ layer **22**, where $0 \leq x \leq 1$, is provided on the AlN barrier layer **20'**. Thus, the AlN barrier layer **20'** is provided on the GaN based layer **18** and disposed between the GaN based layer **18** and the AlGaN based layer **22**.

An optional GaN contact layer or cap layer (not shown) may be provided on the barrier layer **20** to facilitate the formation of contacts of the transistor **10**. An example of such a cap layer is disclosed in U.S. application serial no. 09/904,333 filed July 12, 2001 for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH

ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," which is referenced above. In addition, there may be a compositionally graded transition layer (not shown) between the barrier layer **20** and the contact or cap layer. The source contact **35**, the drain contact **37** and the gate contact **36** may be fabricated as described in U.S. Patent No. 6,316,793.

Figure 2 illustrates the conduction band E_c in the transistor **10** versus height (x). Because of the presence of aluminum in the crystal lattice, AlGaN has a wider bandgap than GaN. Thus, the interface between the channel layer **18** and the barrier layer **20** forms a heterostructure in which the conduction and valence bands E_c and E_v in the barrier layer **20** are offset. Charge is induced due to the piezoelectric effect and spontaneous doping. The conduction band E_c dips below the Fermi level E_f in the area of the channel layer **18** that is immediately adjacent to the barrier layer **20**. Consequently, a two dimensional electron gas (2DEG) sheet charge region **15** is induced at the heterojunction between the channel layer **16** and the barrier layer **20**, while layer **20** is depleted of mobile carriers due to the shape of the conduction band. However, because of the bandgap lineup and arrangement of piezoelectric charge, a similar sheet charge region is not induced at the interface between the channel layer **18** and the bottom confinement layer **16**. Instead, the bottom confinement layer **16** acts to confine mobile carriers in the channel layer **18**, thereby increasing the carrier concentration in the channel layer **18**. Furthermore, by doping a portion of the bottom confinement layer **16** and/or the channel layer **18**, charge at the interface between the bottom confinement layer **16** and the channel layer **18** may be reduced, thereby reducing or eliminating a 2DHG (2D hole gas) region that may form at the interface between the bottom confinement layer **16** and the channel layer **18**.

Electrons in the 2DEG sheet charge region **15** demonstrate high carrier mobility. The conductivity of this region is modulated by applying a voltage to the gate electrode **36**. When a reverse voltage is applied, the conduction band in the vicinity of conduction layer **15** is elevated above the Fermi level, and a portion of the conduction layer **15** is depleted of carriers, thereby preventing the flow of current from the source **35** to the drain **37**.

As discussed above, one shortcoming with conventional HEMT structures is cracking in the AlGaN barrier layer when the layer is grown above a certain critical thickness (which, typically, depends on device geometry, layer structure, growth

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conditions and other factors). It is desirable to have a thick, high Al-composition AlGaN barrier to increase or maximize carrier density in the 2DEG region **15**. One cause of cracking in the barrier layer is accumulated strain energy in the structure. Accordingly, embodiments of the present invention may reduce the overall strain energy in the device by balancing the strain energy components contributed by various layers in the device.

In semiconductor crystal structures, typically, strain effects are present if two different materials are adjacent to one another. As a result, the preferred thickness for an epitaxial layer is a thickness that is appropriate for the other performance parameters of the device, but less than a critical thickness. The critical thickness is, typically, the maximum thickness that the layer can be grown in strained fashion before dislocations or cracks begin to propagate.

The strain ("ε") between two layers is often expressed as the difference in the crystal lattice parameters between the two layers (Δa) divided by the lattice parameter of one of the layers. The higher this strain value, the thinner the layer that can be grown between the two materials. Furthermore, in a multilayer structure such as illustrated in **Figure 1**, the overall strain energy ("Σ") is a function or summation of the individual layer strains, and is referred to as the "effective strain." The overall strain energy or total strain energy may be a linear combination of the strain values or may be a weighted combination of strain energies. For example, the total strain energy may be a weighted sum of the squares of the strain values. Thus, the total strain energy may be proportional to $\sum_i t_i \varepsilon_i^2$ where t_i is the thickness of a layer i.

Strain is generally described as being one of two modes, namely tensile or compressive. Compressive strain of a crystal lattice indicates that the crystal lattice is being compressed into a smaller than usual space, while tensile strain indicates that the crystal lattice is being stretched into a larger than usual space. A crystal lattice can withstand only a certain amount of strain, either compressive or tensile, before the lattice bonds begin to fail and cracks appear in the crystal.

In some embodiments of the present invention, the bottom confinement layer **16** acts as a relaxed or nearly relaxed template to define the strain contributed to the device by the channel layer **18** and barrier layer **20**. Stated differently, the bottom confinement layer **16** is nearly relaxed; thus, the subsequent epitaxial layers of the transistor **10** inherit the lattice constant of bottom confinement layer **16**, and are,

therefore, "pseudomorphically strained" to the extent their lattice constant differs from that of the bottom confinement layer **16**. The channel layer **18** is compressively strained, while the barrier layer **20** is tensile strained, which tends to balance the average or effective strain in the device.

Furthermore, the specific tensile strain and/or compressive strain of the barrier layer **20** and the channel layer **18** may be controlled by, for example, controlling the aluminum concentration in the respective layers.

As described above, the lattice constants of the bottom confinement layer **16**, the channel layer **18** and the barrier layer **20** are substantially the same in the "a" direction (*i.e.* horizontally across the page in **Figure 1**). However, in the "c" direction (*i.e.* vertically or the thickness or growth direction) the lattice constants differ. Thus, strain is induced into the channel layer **18** and the barrier layer **20**. In particular, the unstrained "a" lattice constant of the channel layer **18** is larger than that of the bottom confinement layer **16** and thus, compressive strain is induced in the channel layer **18** as the channel layer **18** attempts to conform to the smaller lattice constant bottom confinement layer **16** on which it is grown. Similarly, the unstrained "a" lattice constant of the channel layer **18** is also larger than that of the barrier layer **20** and thus, tensile strain is induced in the barrier layer **20** as the barrier layer **20** attempts to conform to the larger lattice constant channel layer **18** on which it is grown. While the embodiments illustrated in **Figure 1** are described with regard to particular directions of growth, the present invention should not be construed as limited to such embodiments but may be applied to layers that are coherently strained such that all have the same strained in-plane lattice constant.

In certain embodiments of the present invention, the total strain energy of the transistor **10** is approximately equal to zero. As described above, the total strain energy may be weight average, a non-weighted average, a sum of squares or other such combination of strain energies. Furthermore, the total strain energy may be determined at room temperature. In some embodiments, a non-zero magnitude total strain energy may be provided at a growth temperature such that the total strain energy at room temperature is about zero. Thus, the barrier layer **20** can be grown to a greater thickness than would otherwise be possible for a given amount of strain. As used herein, in some embodiments, the term "approximately zero" total strain energy means a total strain energy of less than a corresponding two layer structure with a lattice mismatch of about 0.1% while in other embodiments, "approximately zero"

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may mean an total strain energy of less than a corresponding two layer structure with a lattice mismatch of about 1%.

In particular embodiments of the present invention, the bottom confinement layer **16** may be $Al_xGa_{1-x}N$, the channel layer **18** may be a GaN layer with a thickness of t_{GaN} and the barrier layer **20** may be $Al_yGa_{1-y}N$ having a thickness of t_y. In such embodiments, the values of x, y and the thicknesses t_{GaN} and t_y may satisfy the equation for linear weighting of strains:

$$x \cong \frac{yt_y}{t_y + t_{GaN}} = \frac{y}{1 + \frac{t_{GaN}}{t_y}}; \text{ or}$$

for weighting of the squares of strains:

$$x \cong \frac{y}{1 + \sqrt{\frac{t_{GaN}}{t_y}}}.$$

Thus, for example, in such embodiments, if the barrier layer **20** and the channel layer **18** have the same thickness then x may be about ½ y.

For example, two SiC wafers were used to grow two different bottom layers, one of the present invention containing an $Al_xGa_{1-x}N$ layer (x~0.1-0.2) and the other using a conventional GaN layer. Upon both of these layers a GaN layer was deposited followed by a high aluminum $Al_xGa_{1-x}N$ layer (x>0.4) with a thickness of 25nm. For the layers grown on GaN layers, the AlGaN was cracked with a crack spacing on the order of only ~1μm preventing any measurement of sheet resistivity. For the layers grown on AlGaN, the AlGaN layer was not cracked, and the sheet resistivity was only 300 Ω/□. This illustrates that the tensile stress in the top AlGaN layer can be effectively reduced to prevent cracking.

In contrast to certain embodiments of the present invention, prior art HEMT structures incorporate a thick relaxed GaN layer as the bottom layer of the device, which then acts as the lattice template for the remaining layers of the device. In such devices, growing a thick, high aluminum percentage AlGaN barrier layer tends to impart too much strain energy to the structure, which can ultimately cause unwanted cracking to occur. An example of a prior art HEMT structure **40** is illustrated in **Figure 3**. HEMT structure **40** includes a substrate **42**, a buffer layer **44**, a GaN channel layer **46** and an AlGaN barrier layer **48** to which source, drain and gate

contacts are made. Because the GaN channel layer **46** serves as the lattice template, the AlGaN barrier layer **48** is tensile strained. As the AlGaN barrier layer **48** is made thicker or the aluminum percentage is increased, the strain energy imparted to the device by the AlGaN barrier layer **48** tends to increase, which can cause cracking as discussed above. Therefore, the thickness of the AlGaN barrier layer **48** may be limited, which in turn limits the achievable carrier density in the channel of the transistor **40**.

Returning to the discussion of the transistor **10** of **Figure 1**, through the use of strain control techniques according to some embodiments of the present invention, the transistor **10** is designed such that, as the layers of the device are being epitaxially deposited, the total strain energy in the structure at no time exceeds a critical level that would cause cracking in the crystal structure. Thus, the strain in the GaN based channel layer **18** is of opposite type to that of the strain in the AlGaN based barrier layer **20** such that the strains substantially offset each other and provide a substantially strain balanced device, thus keeping the strain below a critical threshold where damage occurs to the device. The resulting total strain energy of the device may be compressive or tensile.

In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

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That which is claimed is:

1. A nitride based heterojunction transistor structure, comprising:

a substrate;

a first AlGaN based layer on the substrate, the first AlGaN based layer having a first strain associated therewith;

a GaN based layer on the first AlGaN based layer, the GaN based layer having a bandgap that is less than a bandgap of the first AlGaN based layer and having a second strain associated therewith, the second strain having a magnitude that is greater than a magnitude of the first strain; and

a second AlGaN based layer on the GaN layer opposite the first AlGaN based layer, the second AlGaN based layer having a bandgap that is greater than the bandgap of the GaN based layer and having a third strain associated therewith, the third strain being of opposite strain type to the second strain.

2. The nitride based heterojunction transistor structure according to Claim 1, further comprising a source contact, a drain contact and a gate contact on the second AlGaN based layer.

3. The nitride based heterojunction transistor structure according to Claim 1, further comprising an AlN layer on the GaN based layer and disposed between the GaN based layer and the second AlGaN based layer.

4. The nitride based heterojunction transistor structure according to Claim 1, wherein the first AlGaN based layer comprises a short period super-lattice of AlN based layers and GaN based layers.

5. The nitride based heterojunction transistor structure of Claim 4, wherein the AlN based layers and the GaN based layers of the short period super-lattice comprise AlN layers and GaN layers respectively.

6. The nitride based heterojunction transistor structure of Claim 1, wherein the second AlGaN based layer comprises an $Al_xGa_{1-x}N$ layer, where $0 < x \leq 1$.

7. The nitride based heterojunction transistor structure of Claim 1, wherein the first AlGaN based layer comprises a bottom confinement layer, the GaN layer comprises a channel layer and the second AlGaN based layer comprises a barrier layer.

8. The nitride based heterojunction transistor structure of Claim 7, wherein the bottom confinement layer has a first aluminum concentration and the barrier layer has a second aluminum concentration different from the first aluminum concentration.

9. The nitride based heterojunction transistor structure of Claim 8, wherein the second aluminum concentration is greater than the first aluminum concentration.

10. The nitride based heterojunction transistor structure of Claim 1, wherein the second AlGaN based layer has a thickness and aluminum concentration large enough to induce formation of a 2D electron gas at the interface with the GaN based layer, but less than a thickness at which cracking or defect formation occurs.

11. The nitride based heterojunction transistor structure of Claim 1, wherein the second AlGaN layer has a thickness of at least about 10 nm.

12. The nitride based heterojunction transistor structure of Claim 1, wherein a total strain energy in the first AlGaN based layer, the GaN based layer and the second AlGaN based layer is about zero.

13. The nitride based heterojunction transistor structure of Claim 12, wherein the total strain energy comprises a weighted sum of strains of layers of the heterojunction transistor.

14. The nitride based heterojunction transistor structure of Claim 1, wherein a total strain energy in the first AlGaN based layer, the GaN based layer and the second AlGaN based layer at room temperature is approximately zero.

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15. The nitride based heterojunction transistor structure of Claim 14, wherein a magnitude of the total strain energy is greater than approximately zero at a growth temperature.

16. The nitride based heterojunction transistor structure of Claim 1, wherein the first AlGaN based layer, the GaN layer and the second AlGaN based layer are coherently strained such that all have the same strained in-plane lattice constant .

17. The nitride based heterojunction transistor structure of Claim 1, further comprising a buffer layer between the substrate and the first AlGaN based layer.

18. The nitride based heterojunction transistor structure of Claim 17, wherein the buffer layer comprises an AlN layer.

19. The nitride based heterojunction transistor structure of Claim 1, wherein the GaN based layer is directly on the first AlGaN based layer.

20. The nitride based heterojunction transistor structure of Claim 19, wherein the second AlGaN based layer is directly on the GaN based layer.

21. The nitride based heterojunction transistor structure of Claim 1, wherein the first AlGaN based layer is a graded AlGaN based layer.

22. The nitride based heterojunction transistor structure of Claim 1, wherein the first AlGaN based layer is an AlGaN layer.

23. The nitride based heterojunction transistor structure of Claim 1, wherein the first AlGaN based layer is an AlInGaN layer.

24. The nitride based heterojunction transistor structure of Claim 1, wherein the first AlGaN based layer has an aluminum percentage of greater than about 10%.

25. The nitride based heterojunction transistor structure of Claim 1, wherein the second AlGaN based layer has an aluminum percentage of greater than about 20%.

26. The nitride based heterojunction transistor structure of Claim 1, wherein the first AlGaN based layer has thickness of at least about 1000nm.

27. The nitride based heterojunction transistor structure of Claim 1, wherein the GaN based layer has a thickness of from about 30 Å to about 300 Å.

28. The nitride based heterojunction transistor structure of Claim 1, wherein the GaN based layer has a thickness of greater than about 500 Å.

29. The nitride based heterojunction transistor structure of Claim 1, wherein the substrate comprises a silicon carbide substrate.

30. A method of fabricating a nitride based heterojunction transistor structure, comprising:

forming a substantially unstrained AlGaN based layer on a substrate;

forming a compressive strained GaN based layer on the substantially unstrained AlGaN based layer; and

forming a tensile strained AlGaN based layer on the compressive strained GaN based layer.

31. The method of Claim 30, wherein the step of forming a tensile strained AlGaN based layer comprises the step of forming a tensile strained AlGaN based layer having a predefined tensile strain on the compressive strained GaN based layer, the predefined tensile strain providing a tensile strain such that an total strain energy of the compressive strained GaN based layer and the tensile strained AlGaN based layer is about zero.

32. The method of Claim 31, wherein the predefined tensile strain is provided by adjusting at least one of a thickness of the tensile strained AlGaN based

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layer, a composition of the substantially unstrained AlGaN based layer and/or an aluminum concentration in the tensile strained AlGaN based layer to provide the predefined tensile strain.

33. The method of Claim 31, wherein the total strain energy comprises a linear summation of strain energies.

34. The method of Claim 31, wherein the total strain energy comprises a weighted summation of strain energies.

35. The method of Claim 31, wherein the total strain energy comprises a weighted sum of squares of the strain energy.

36. The method of Claim 30, wherein the step of forming a substantially unstrained AlGaN based layer comprises the steps of:

forming three dimensional islands of AlGaN based material on the substrate; and

growing the AlGaN based material so that the AlGaN based material coalesces between the three dimensional islands to provide the substantially unstrained AlGaN based layer.

37. The method of Claim 30, wherein the step of forming a substantially unstrained AlGaN based layer comprises forming a substantially unstrained AlGaN layer.

38. The method of Claim 30, wherein the step of forming a substantially unstrained AlGaN based layer comprises forming a substantially unstrained short period super-lattice of AlN and GaN based layers.

39. The method of Claim 30, wherein the step of forming a substantially unstrained AlGaN based layer comprises forming a substantially unstrained short period super-lattice of AlN and GaN layers.

40. The method of Claim 30, wherein the step of forming a substantially unstrained AlGaN based layer comprises forming a substantially unstrained AlInGaN layer.

41. The method of Claim 30, further comprising the step of forming a tensile strained AlN layer on the GaN based layer and disposed between the GaN based layer and the tensile strained AlGaN based layer.

42. The method of Claim 30, wherein the step of forming a tensile strained AlGaN based layer comprises forming a tensile strained AlGaN layer.

43. The method of Claim 30, wherein the step of forming a tensile strained AlGaN based layer comprises forming a tensile strained AlInGaN layer.

44. The method of Claim 30, wherein the step of forming a tensile strained AlGaN based layer comprises forming a tensile strained AlGaN based layer having a thickness of at least 10 nm.

45. The method of Claim 30, wherein the step of forming a compressive strained GaN based layer comprises forming a compressive strained GaN based layer having a thickness of from about 30 Å to about 300 Å.

46. The method of Claim 30, wherein the step of forming a compressive strained GaN based layer comprises forming a compressive strained GaN based layer having a thickness of greater than about 500 Å.

47. The method of Claim 30, wherein the step of forming a substantially unstrained AlGaN based layer comprises forming a substantially unstrained AlGaN based layer having a first aluminum concentration and the step of forming a tensile strained AlGaN based layer comprises forming a tensile strained AlGaN based layer having a second aluminum concentration different from the first aluminum concentration.

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48. The method of Claim 47, wherein the second aluminum concentration is greater than the first aluminum concentration.

49. The method of Claim 30, wherein the step of forming a tensile strained AlGaN based layer comprises forming a tensile strained AlGaN based layer having a thickness and aluminum concentration large enough to induce formation of a 2D electron gas at the interface with the compressive strained GaN based layer, but less than a thickness at which cracking or defect formation occurs.

50. A nitride based heterojunction transistor, comprising:
an AlGaN based bottom confinement layer;
a GaN based channel layer on the bottom confinement layer; and
an AlGaN based barrier layer on the channel layer opposite the bottom confinement layer, the barrier layer having a higher concentration of aluminum than the bottom confinement layer.

51. The nitride based heterojunction transistor of Claim 50, wherein the channel layer has a thickness of from about 30 Å to about 300 Å.

52. The nitride based heterojunction transistor of Claim 50, wherein the barrier layer has a thickness of at least about 10 nm.

53. The nitride based heterojunction transistor of Claim 50, wherein the bottom confinement layer is on a silicon carbide substrate.

54. The nitride based heterojunction transistor of Claim 53, further comprising an AlN buffer layer between the silicon carbide substrate and the bottom confinement layer.

55. The nitride based heterojunction transistor of Claim 50, wherein the bottom confinement layer is a graded AlGaN based layer.

56. The nitride based heterojunction transistor of Claim 50 further comprising a GaN based contact layer on the barrier layer.

57. The nitride based heterojunction transistor of Claim 50, wherein the bottom confinement layer has an aluminum concentration of greater than about 10%.

58. The nitride based heterojunction transistor of Claim 50, wherein the barrier layer has an aluminum concentration of greater than about 20%.

59. The nitride based heterojuntion transistor of Claim 50, further comprising an AlN based layer on the GaN based layer and disposed between the GaN based channel layer and the AlGaN based barrier layer.

60. A method of fabricating a nitride based heterojunction transistor, comprising:

forming an AlGaN based bottom confinement layer on a substrate;

forming a GaN based channel layer on the bottom confinement layer; and

forming an AlGaN based barrier layer on the channel layer, the barrier layer having a higher concentration of aluminum than the bottom confinement layer.

61. The method of Claim 60, wherein the channel layer is formed to a thickness of from about 30 Å to about 300 Å.

62. The method of Claim 60, wherein the barrier layer is formed to a thickness of at least about 10 nm.

63. The method of Claim 60, wherein the step of forming an AlGaN based bottom confinement layer comprises forming an AlGaN based bottom confinement layer on a silicon carbide substrate.

64. The method of Claim 63, further comprising forming an AlN buffer layer on the silicon carbide substrate and wherein the step of forming an AlGaN based bottom confinement layer comprises forming an AlGaN based bottom confinement layer on the buffer layer.

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65. The method of Claim 60, wherein the step of forming an AlGaN based bottom confinement layer comprises forming a graded AlGaN based layer.

66. The method of Claim 60 further comprising forming a GaN based contact layer on the barrier layer.

67. The method of Claim 60, wherein the bottom confinement layer has an aluminum concentration of greater than about 10%.

68. The method of Claim 60, wherein the barrier layer has an aluminum concentration of greater than about 20%.

69. The method of Claim 60, further comprising the step of forming an AlN layer on the GaN based layer and disposed between the GaN based channel layer and the AlGaN based barrier layer.

70. A Group III-nitride based heterojunction transistor structure, comprising:

a substrate;

a first Group III-nitride based layer on the substrate, the first Group III-nitride based layer having a first strain associated therewith;

a second Group III-nitride based layer on the first Group III-nitride based layer, the second Group III-nitride based layer having a bandgap that is less than a bandgap of the first Group III-nitride based layer and having a second strain associated therewith, the second strain having a magnitude that is greater than a magnitude of the first strain; and

a third Group III-nitride based layer on the second Group III-nitride based layer opposite the first Group III-nitride based layer, the third Group III-nitride based layer having a bandgap that is greater than the bandgap of the second Group III-nitride based layer and having a third strain associated therewith, the third strain being of opposite strain type to the second strain.

71. The Group III nitride based heterojunction transistor structure according to Claim 70, wherein the first Group III-nitride based layer comprises an $Al_xGa_{1-x}N$ layer, where $0 < x < 1$.

72. The Group III nitride based heterojunction transistor structure according to Claim 71, wherein the second Group III-nitride based layer comprise a GaN layer.

73. The Group III nitride based heterojunction transistor structure according to Claim 72, wherein the third Group III-nitride base layer comprises an AlN layer.

74. A method of fabricating a Group III-nitride based heterojunction transistor structure, comprising:

forming a first Group III-nitride based layer on a substrate, the first Group III-nitride based layer having a first strain associated therewith;

forming a second Group III-nitride based layer on the first Group III-nitride based layer, the second Group III-nitride based layer having a bandgap that is less than a bandgap of the first Group III-nitride based layer and having a second strain associated therewith, the second strain having a magnitude that is greater than a magnitude of the first strain; and

forming a third Group III-nitride based layer on the second Group III-nitride based layer opposite the first Group III-nitride based layer, the third Group III-nitride based layer having a bandgap that is greater than the bandgap of the second Group III-nitride based layer and having a third strain associated therewith, the third strain being of opposite strain type to the second strain.

75. The method of Claim 74, wherein the step of forming a first Group III-nitride based layer comprises forming an $Al_xGa_{1-x}N$ layer, where $0 < x < 1$.

76. The method of Claim 75, wherein the step of forming a second Group III-nitride based layer comprises forming a GaN layer.

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77. The method of Claim 76, wherein the step of forming a third Group III-nitride based layer comprises forming an AlN layer.

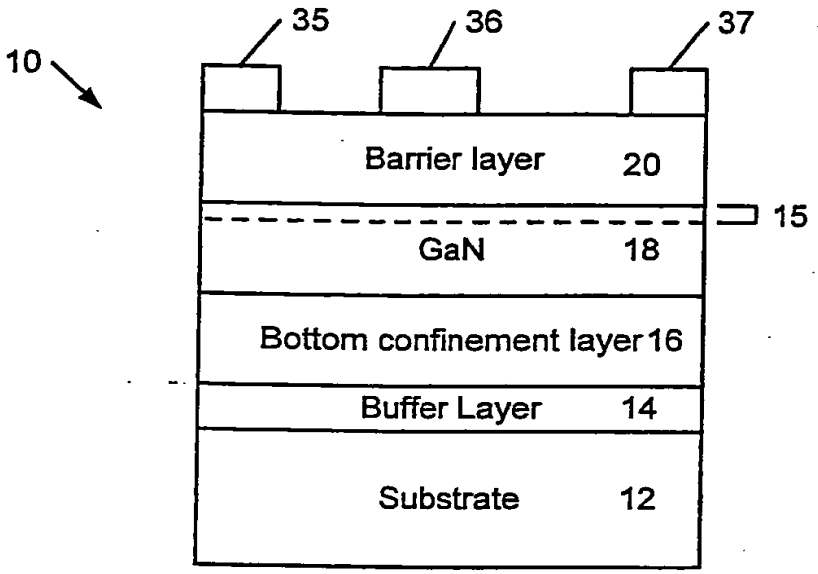

Figure 1

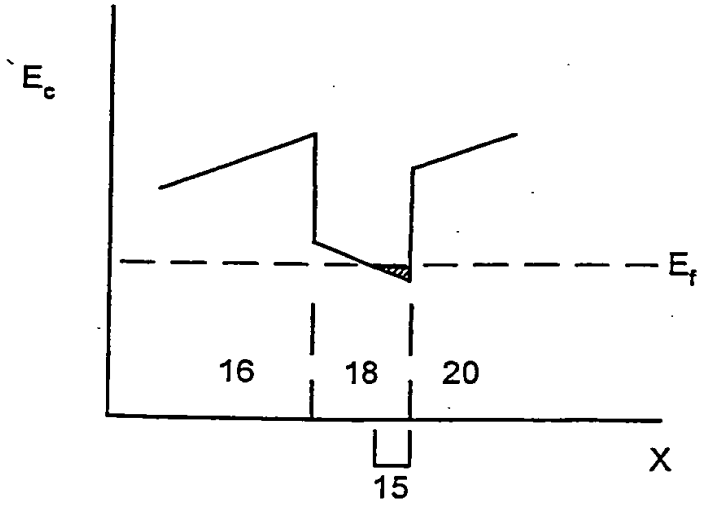

Figure 2

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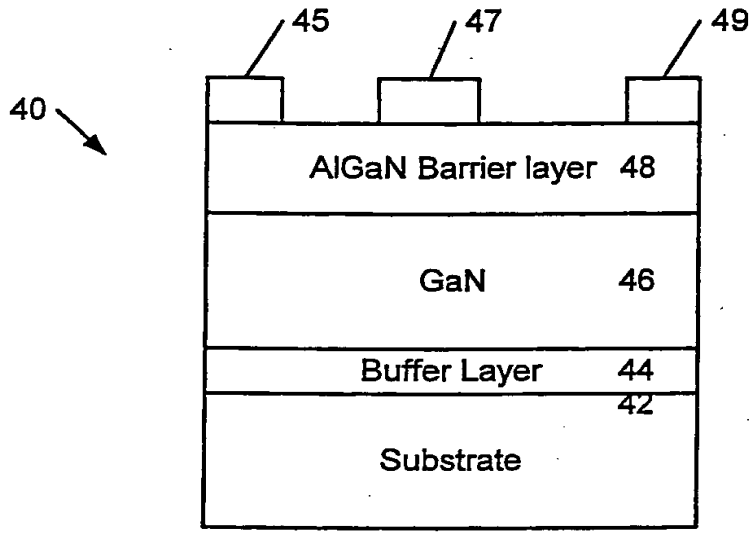

Figure 3

PRIOR ART

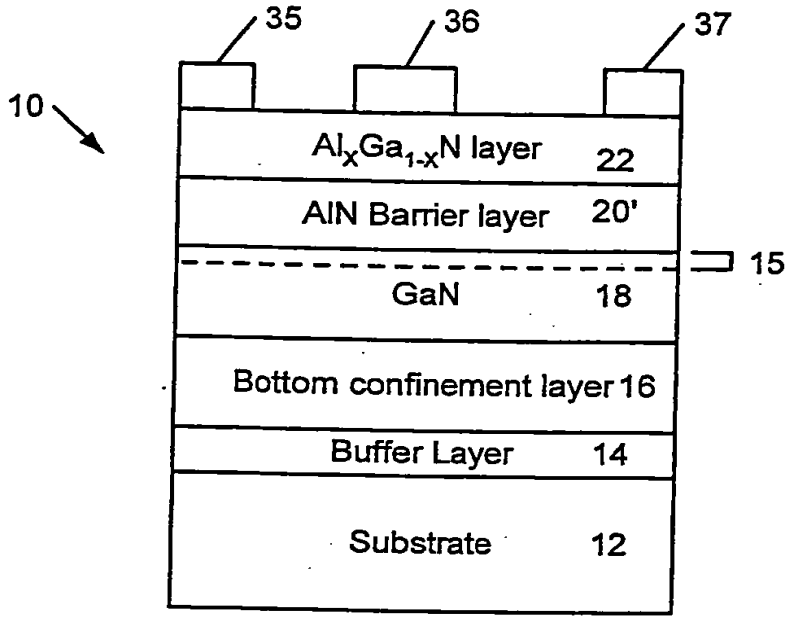

Figure 4

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/37244

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/778 H01L29/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	US 2001/015446 A1 (INOUE KAORU ET AL) 23 August 2001 (2001-08-23) page 6, column 1, paragraph 72; figure 7	1-77
A	US 2001/023964 A1 (WU YIFENG ET AL) 27 September 2001 (2001-09-27) figure 1	1-77
A	US 6 064 082 A (KOBAYASHI TOSHIMASA ET AL) 16 May 2000 (2000-05-16) figure 4	1-77

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 March 2003	04/04/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax (+31–70) 340–3016	Juhl, A

INTERNATIONAL SEARCH REPORT

Interna l Application No
PCT/US 02/37244

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 192 987 A (KHAN MUHAMMED A ET AL) 9 March 1993 (1993-03-09) cited in the application figures 1,5	1-77
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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US 02/37244

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